Electronic Version
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Claims

[c1] 1. A memory device, comprising:

a plurality of isolation structures disposed in a substrate, defining a plurality of active regions in the substrate;

a plurality of pairs of word lines, substantially parallel to one another, disposed on and in a direction vertical to the plurality of the isolation structures and the plurality of the active regions, wherein the active regions that are covered by the plurality of pairs of the word lines are defined as a plurality of first channel regions;

a plurality of first gates disposed on the plurality of the first channel regions and between the substrate and the plurality of word lines;

a plurality of pairs of source lines, substantially parallel to the plurality of pairs of the word lines, each pair of source lines being between each pair of word lines, wherein the plurality of the source lines are disposed in a direction vertical to the plurality of the isolation structures and the plurality of the active regions, and wherein the active regions that are covered by the plurality of pairs of the source lines are defined as a plurality of second channel regions;

a plurality of second gates, in strip shapes, disposed on

and in a direction vertical to the plurality of the isolation structures and the plurality of the active regions and between the substrate and the plurality of the source lines;
a first dielectric layer disposed between the plurality of the active regions and the plurality of the first gates, and between the plurality of the active regions and the plurality of the second gates;
a second dielectric layer disposed between the plurality of the word lines and the plurality of the first gates, and between the plurality of the source lines and the plurality of the second gates;
a third dielectric layer disposed over the substrate and covering the plurality of the word lines and the plurality of the source lines;
a plurality of source/drain regions disposed in the active regions beside the first gates and the second gates;
a plurality of source line contacts, through the third dielectric layer, connecting to the source/drain regions that are between each pair of the source lines and electrically connecting to at least one of each pair of the source lines; and
a plurality of insulating layers disposed between the plurality of the second gates and the plurality of the source line contacts.

[c2] 2. The memory device of claim 1, wherein the plurality of

the isolation structures, substantially parallel to one another, are disposed in the substrate and are in strip shapes, thus defining the plurality of active regions in strip shapes.

[c3] 3. The memory device of claim 1, wherein a height of the source lines disposed above the second gates is between a height of the second gates and a height of the word lines.

[c4] 4. The memory device of claim 3, wherein the height of the source lines disposed above the second gates is substantially the same as the height of the word lines.

[c5] 5. The memory device of claim 1, wherein a material of the source lines is the same as that of the word lines.

[c6] 6. The memory device of claim 1, wherein a material of the source lines includes polysilicon and metal silicide, while a material of the word lines includes polysilicon and metal silicide.

[c7] 7. The memory device of claim 1, further comprising a plurality of spacers, disposed between the word lines and the source lines neighboring to the word lines, and wherein a thickness of the insulating layer between the second gate and the source line contact is smaller than a half of a thickness of the spacer.

[c8] 8. The memory device of claim 1, wherein each source line contact connects to one source/drain region in one active region between each pair of the source lines and connects to at least one of each pair of the source lines.

[c9] 9. The memory device of claim 1, wherein each source line contact connects to at least two source/drain regions in at least two adjacent active regions between each pair of the source lines and connects to at least one of each pair of the source lines.

[c10] 10. The memory device of claim 1, wherein each source line contact is a self-aligned contact.

[c11] 11. The memory device of claim 1, further comprising a plurality of bit line contacts, through the third dielectric layer, connecting the source/drain regions beside each pair of the word lines, and wherein a height of the bit line contacts is substantially the same as a height of the source line contacts.

[c12] 12. The memory device of claim 1, wherein when the memory device is a flash memory device, the first gate is a floating gate and the second gate is a select gate.

[c13] 13. A memory device, disposed in a substrate, the memory device comprising a plurality of pairs of word lines, a

plurality of pairs of source lines and a plurality of source/drain regions, wherein the memory device is characterized in that:
each pair of source lines, substantially parallel to each other and electrically connected to each other, is disposed between each pair of word lines, and the source/drain regions are disposed between each pair of source lines and between the source lines and the adjacent word lines, the word lines, the source lines and the source/drain regions are covered by a dielectric layer; and
a plurality of source line contacts, through the third dielectric layer, is further included, connecting to at least one of the source/drain regions that are between each pair of the source lines and electrically connecting to at least one of each pair of the source lines.

[c14] 14. The memory device of claim 13, wherein a height and a contour of the source lines are substantially equivalent to a height and a contour of the word lines.

[c15] 15. The memory device of claim 13, wherein a material of the source lines is the same as a material of the word lines.

[c16] 16. The memory device of claim 15, wherein the material of the source lines includes polysilicon and metal silicide, while the material of the word lines includes

polysilicon and metal silicide.

[c17] 17. The memory device of claim 13, wherein the memory device is further characterized in that:
a plurality of isolation structures is disposed in the substrate and is in strip shapes, thus defining a plurality of active regions in strip shapes in the substrate; and
each source line contact connects to one source/drain region in one active region between each pair of the source lines and connects to at least one of each pair of the source lines.

[c18] 18. The memory device of claim 13, wherein the memory device is further characterized in that:
a plurality of isolation structures is disposed in the substrate and is in strip shapes, thus defining a plurality of active regions in strip shapes in the substrate; and
each source line contact connects to at least two source/drain regions in at least two adjacent active regions between each pair of the source lines and connects to at least one of each pair of the source lines.

[c19] 19. The memory device of claim 13, wherein each source line contact is a self-aligned contact.

[c20] 20. The memory device of claim 13, further comprising a plurality of bit line contacts, through the third dielectric

layer, connecting the source/drain regions beside each pair of the word lines, and wherein a height of the bit line contacts is substantially the same as a height of the source line contacts.

[c21] 21. The memory device of claim 17, further comprising:
a plurality of first gates, disposed between the substrate and the word lines;
a plurality of second gates, in strip shapes, disposed on and in a direction vertical to the plurality of the strip isolation structures and the plurality of the active regions and disposed between the substrate and the source lines;
a first dielectric layer, disposed between the substrate and the plurality of the fist gates and between the substrate and the plurality of the second gates; and
a second dielectric layer, disposed between the plurality of the fist gates and the word lines and between the source lines and the plurality of the second gates.

[c22] 22. The memory device of claim 21, wherein when the memory device is a flash memory device, the first gate is a floating gate and the second gate is a select gate.

[c23] 23. A method for fabricating a memory device disposed in a substrate, the memory device comprising a plurality of pairs of word lines, a plurality of pairs of source lines

and a plurality of source/drain regions, wherein the method for fabricating the memory device is characterized in that:
forming one pair of source lines that are electrically connected to each other between each pair of word lines, so that the source/drain regions are disposed beside each word line and each source line;
forming a dielectric layer over the substrate; and
forming a plurality of source line contacts, one source line contact being in the dielectric layer between each pair of the source lines, wherein each source/drain region between each pair of the source lines is electrically connected to at least one of each pair of the source lines by each source line contact.

[c24] 24. The method of claim 23, wherein the method is further characterized in that:
the word lines and the source lines are formed by patterning a same conductive layer.

[c25] 25. The method of claim 23, further comprising forming a plurality of bit line contacts in the dielectric layer, wherein the method is further characterized in that:
forming a plurality of source line contact openings and a plurality of bit line contact openings in the dielectric layer in a same process of photolithography and etching; and

filling a conductive layer into the plurality of source line contact openings and the plurality of bit line contact openings to form the plurality of source line contacts and the plurality of bit line contacts.

[c26] 26. The method of claim 23, further comprising forming a plurality of bit line contacts in the dielectric layer, wherein the method is further characterized in that:
forming a plurality of source line contact openings in the dielectric layer in a first process of photolithography and etching
forming a plurality of bit line contact openings in the dielectric layer in a second process of photolithography and etching; and
filling a conductive layer into the plurality of source line contact openings and the plurality of bit line contact openings to form the plurality of source line contacts and the plurality of bit line contacts.

[c27] 27. The method of claim 23, wherein the plurality of source line contacts is formed by forming a plurality of source line contact openings in the dielectric layer and then filling a conductive material into the plurality of source line contact openings, the method is further characterized in that:
each source line contact opening is a self-aligned contact opening, and the method further comprising:

forming a conformal etching stop layer over the substrate, after forming the dielectric layer and before forming the plurality of self-aligned source line contact openings, and the step of forming the plurality of source line contact openings in the dielectric layer further comprising:

removing the dielectric layer covering the source/drain regions between each pair of source lines using the conformal etching stop layer as a stop layer, and at least removing the dielectric layer covering at least one of each pair of source lines, to form the plurality of the self-aligned source line contact openings; and

etching back the conformal etching stop layer exposed by the source line contact openings to expose the source/drain regions and at least expose one of each pair of source lines.

[c28] 28. The method of claim 23, further comprising forming a plurality of spacers on sidewalls of the word lines and the source lines, after forming the word lines and the source lines and before forming the dielectric layer, the method is further characterized in that:

forming a liner layer on the sidewalls of the word lines and the source lines before forming the spacers, and further comprising removing the spacers between each pair of the source lines to expose the liner layer after the

step of forming the spacers.

[c29] 29. The method of claim 23, wherein the method is further characterized in that:
forming a plurality of isolation structures in strip shapes in the substrate, thus defining a plurality of active regions in strip shapes in the substrate, wherein the active regions are not connected to one another, and wherein the word lines are disposed in a direction vertical to the strip isolation structures and the strip active regions.

[c30] 30. A method for fabricating a memory device, comprising:
forming a plurality of strip isolation structures in a substrate to define a plurality of strip active regions in the substrate, wherein the plurality of the strip active regions includes a plurality of pairs of first channel regions in arrays and a plurality of pairs of second channel regions in arrays, and wherein each pair of the second channel regions are disposed between each pair of the first channel regions;
forming a first dielectric layer on the substrate;
forming a plurality of first gates and a plurality of strip second gates simultaneously, each first gate being disposed on the first dielectric layer above each first channel region and each strip second gate being disposed on the first dielectric layer above each second channel re-

gion and the strip isolation structures;
forming a plurality of second dielectric layers, one of the second dielectric layers disposed on each first gate and on each strip second gate;
forming a first conductive layer over the substrate;
defining the first conductive layer to form a plurality of pairs of word lines and a plurality of pairs of source lines, wherein the word lines and the source lines are disposed in a direction vertical to the strip isolation structures and the strip active regions, while each pair of source lines are disposed between each pair of the word lines, and wherein each word line covers the second dielectric layers on the first channel regions of the same row and each source line covers the second dielectric layers on the second channel regions of the same row;
forming a plurality of source/drain regions in the substrate beside the word lines and the source lines;
forming a spacer on each sidewall of each word line and on each sidewall of each source line;
forming a third dielectric layer over the substrate;
forming a plurality of source line contact openings in the third dielectric layer, exposing the source/drain regions that are between each pair of source lines and at least exposing one of each pair of the source lines; and
filling a conductive material into the source line contact openings to form a plurality of source line contacts for

connecting the source/drain regions that are between each pair of source lines and at least connecting one of each pair of the source lines.

[c31] 31. The method of claim 30, further comprising forming a conformal etching stop layer over the substrate before the step of forming the third dielectric layer and after the step of forming the spacer, wherein each source line contact opening is a self-aligned contact opening, and wherein the step of forming the source line contact openings further comprises:
removing the third dielectric layer covering the source/drain regions between each pair of source lines using the conformal etching stop layer as a stop layer, and at least removing the third dielectric layer covering at least one of each pair of source lines, to form the plurality of the self-aligned source line contact openings; and
etching back the conformal etching stop layer exposed by the source line contact openings to expose the source/drain regions and at least expose one of each pair of source lines.

[c32] 32. The method of claim 30, further comprising forming a liner layer on the sidewalls of the word lines and the source lines, after the step of forming the word lines and the source lines and before the step of forming the spacers, and further comprising removing the spacers

between each pair of the source lines to expose the liner layer after the step of forming the spacers.

[c33] 33. The method of claim 30, further comprising forming a conformal etching stop layer over the substrate after the step of removing the spacers and before the step of forming the source line contact openings in the third dielectric layer, wherein each source line contact opening is a self-aligned contact opening, and wherein the step of forming the source line contact openings further comprises:

removing the third dielectric layer covering the source/drain regions between each pair of source lines using the conformal etching stop layer as a stop layer, and at least removing the third dielectric layer covering at least one of each pair of source lines, to form the plurality of the source line contact openings; and

etching back the conformal etching stop layer exposed by the source line contact openings to expose the source/drain regions and at least expose one of each pair of source lines.

[c34] 34. The method of claim 30, wherein each source line contact exposes one source/drain region in one strip active region between each pair of the source lines and exposes at least one of each pair of the source lines.

[c35] 35. The method of claim 30, wherein each source line contact exposes at least two source/drain regions in at least two adjacent active regions between each pair of the source lines and exposes at least one of each pair of the source lines.

[c36] 36. The method of claim 30, further comprising:
forming a plurality of bit line contact openings in the third dielectric layer, so that each bit line contact opening exposes one source/drain region beside each pair of the word lines; and
filling a conductive material into the bit line contact openings to form a plurality of bit line contacts, wherein each bit line contact connects to one source/drain region beside each pair of the word lines.

[c37] 37. The method of claim 36, wherein the plurality of source line contact openings and the bit line contact openings are formed at the same time.

[c38] 38. The method of claim 36, wherein the plurality of source line contact openings and the bit line contact openings are not formed at the same time.

[c39] 39. The method of claim 30, wherein the step of the plurality of first gates and the plurality of strip second gates comprises:

forming a second conductive layer over the substrate;
defining the second conductive layer to form a patterned second conductive layer having a plurality of openings, wherein the opening is disposed between the adjacent strip active regions; and
after forming the second dielectric layer and the first conductive layer, defining the second conductive layer at the same time as defining the first conductive layer strip, to form the plurality of the first gates and the plurality of strip second gates, wherein the first gates on the active regions of the same row are separated from each other by the openings.